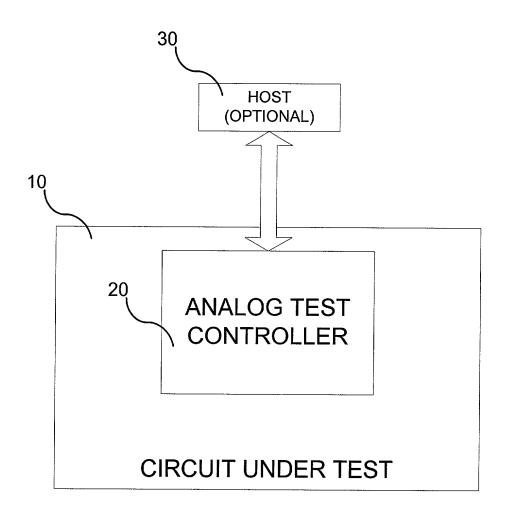
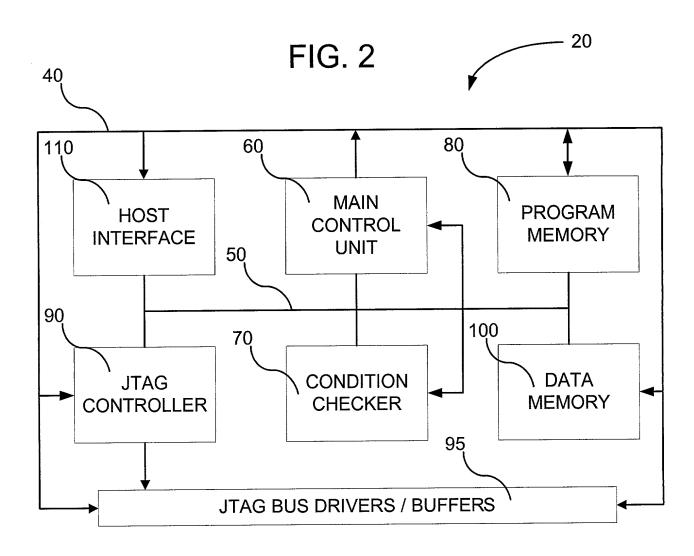
Inventor: Mohammed Ali AbdEl-Halim AbdEl-Wahid
Express Mail No.: EL874429377US / Date of Deposit: October 26, 2001
Title: DESIGN FOR TEST OF ANALOG MODULE SYSTEMS
Attorney's Matter No.: 1011-59137/RFS
Page 1 of 14

FIG. 1

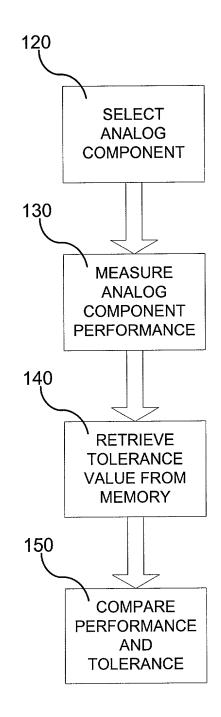


Inventor: Mohammed Ali AbdEl-Halim AbdEl-Wahid
Express Mail No.: EL874429377US / Date of Deposit: October 26, 2001
Title: DESIGN FOR TEST OF ANALOG MODULE SYSTEMS
Attorney's Matter No.: 1011-59137/RFS
Page 2 of 14



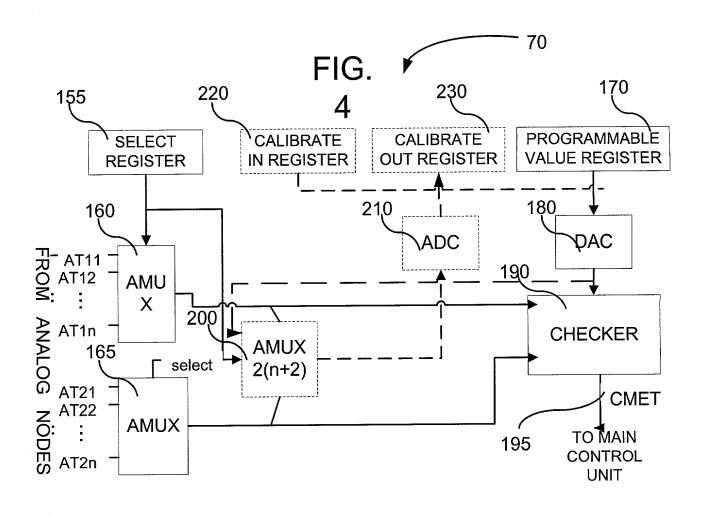
Inventor: Mohammed Ali AbdEl-Halim AbdEl-Wahid Express Mail No.: EL874429377US / Date of Deposit: October 26, 2001 Title: DESIGN FOR TEST OF ANALOG MODULE SYSTEMS Attorney's Matter No.: 1011-59137/RFS Page 3 of 14

FIG. 3

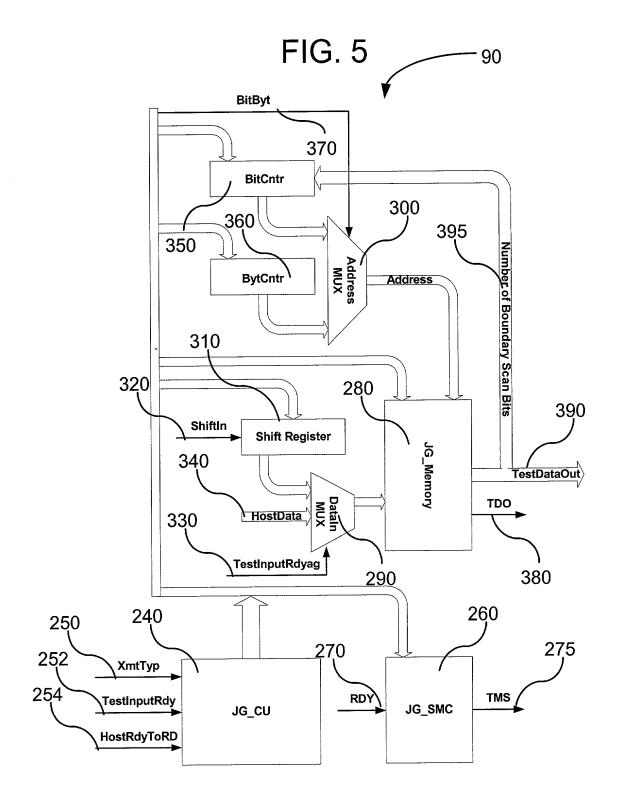


Inventor: Mohammed Ali AbdEl-Halim AbdEl-Wahid Express Mail No.: EL874429377US / Date of Deposit: October 26, 2001 Title: DESIGN FOR TEST OF ANALOG MODULE SYSTEMS Attorney's Matter No.: 1011-59137/RFS

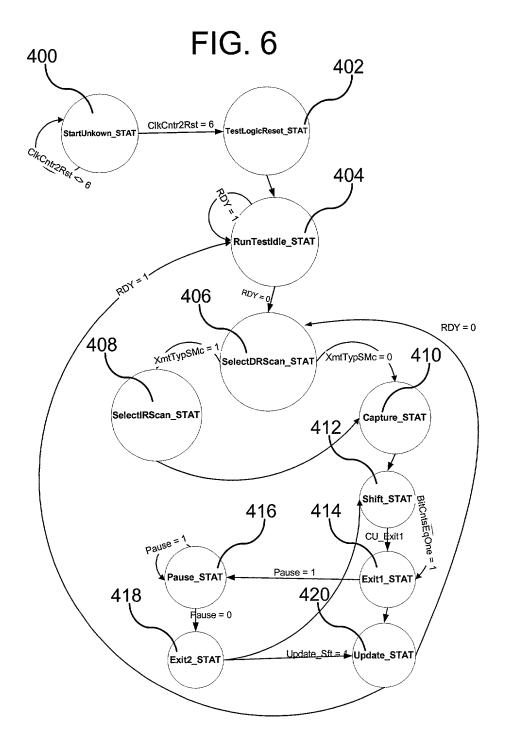
Page 4 of 14



Inventor: Mohammed Ali AbdEl-Halim AbdEl-Wahid
Express Mail No.: EL874429377US / Date of Deposit: October 26, 2001
Title: DESIGN FOR TEST OF ANALOG MODULE SYSTEMS
Attorney's Matter No.: 1011-59137/RFS
Page 5 of 14



Inventor: Mohammed Ali AbdEl-Halim AbdEl-Wahid
Express Mail No.: EL874429377US / Date of Deposit: October 26, 2001
Title: DESIGN FOR TEST OF ANALOG MODULE SYSTEMS
Attorney's Matter No.: 1011-59137/RFS
Page 6 of 14



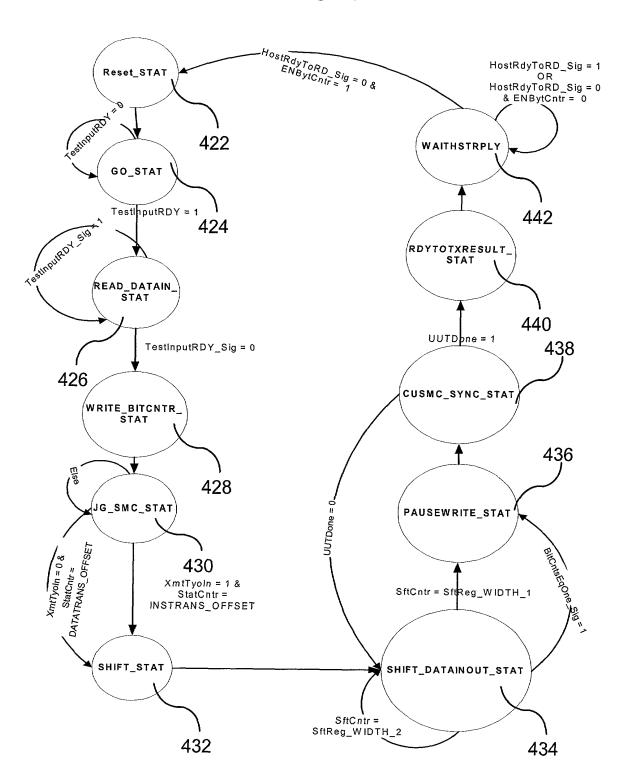
Inventor: Mohammed Ali AbdEl-Halim AbdEl-Wahid
Express Mail No.: EL874429377US / Date of Deposit: October 26, 2001
Title: DESIGN FOR TEST OF ANALOG MODULE SYSTEMS
Attorney's Matter No.: 1011-59137/RFS
Page 7 of 14

FIG. 6a

			OUTPUT					
	R D Y	X m t T y p S M	CU EXIT1	BitCntsEqOn	Paus	U p d a t e S f t	C I k C n t r 2 R s t	TMS
STATE	T	С		е	е	<u> </u>		TWO
StartUnknown_STAT	Х	Х	Х	Х	Х	Х	Х	1
TestLogicReset_STAT	Х	Х	Х	Х	Х	Х	Х	0
RunTestIdle_STAT	1	Х	Х	Х	Х	Х	Х	0
RunTestIdle_STAT	0	Х	Х	Х	Х	Х	Х	11
SelectDRScan_STAT	Х	1	Х	Х	Х	Х	Х	1
SelectDRScan_STAT	Х	0	Х	X	Х	Х	Х	0
SelectiRScan_STAT	Х	Х	Х	Х	Х	Х	Х	0
Capture_STAT	Х	Х	Х	X	Х	Х	X	0
Shift_STAT	Х	Х	1	Х	X	X	X	1
Shift_STAT	Х	Х	Х	1	Х	Х	Х	1
Shift_STAT	Х	Х	0	0	Х	Х	Х	0
Exit1_STAT	Х	Х	Х	Х	0	Х	Х	1
Exit1_STAT	Х	Х	Х	Х	1	Х	Х	0
Pause_STAT	Х	Х	Х	Х	0	X	Х	1
Pause_STAT	Х	Х	Х	Х	1	X	Х	0
Exit2_STAT	Х	Х	Х	Х	Х	1	Х	1
Exit2_STAT	Х	Х	Х	Х	Х	0	X	0
Update_STAT	0	Х	Х	Х	Х	X	Х	11
Update_STAT	1	Х	Х	X	X	Х	X	0

Inventor: Mohammed Ali AbdEl-Halim AbdEl-Wahid Express Mail No.: EL874429377US / Date of Deposit: October 26, 2001 Title: DESIGN FOR TEST OF ANALOG MODULE SYSTEMS Attorney's Matter No.: 1011-59137/RFS Page 8 of 14

FIG. 7

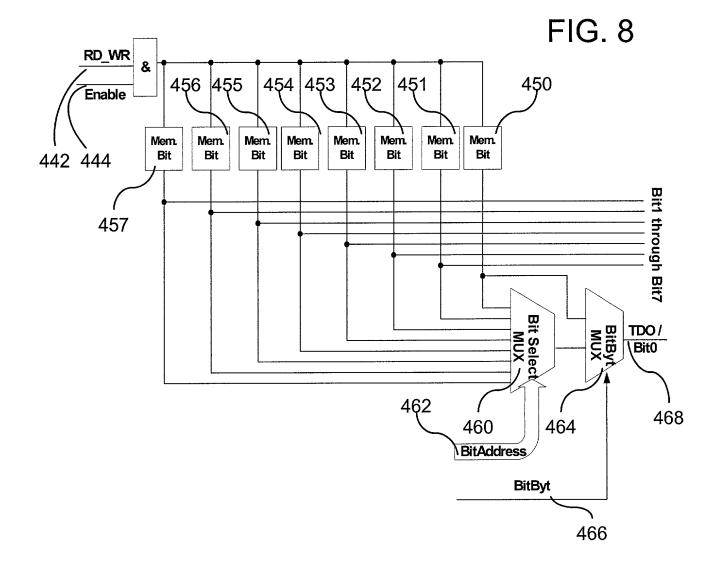


Inventor: Mohammed Ali AbdEl-Halim AbdEl-Wahid Express Mail No.: EL874429377US / Date of Deposit: October 26, 2001 Title: DESIGN FOR TEST OF ANALOG MODULE SYSTEMS Attorney's Matter No.: 1011-59137/RFS
Page 9 of 14

FIG. 7A

	mzo+	. a + O =	ъ.	S :- 5	0	0	0	-	0	0	1	0	0	, 0	0	0	0	0	0	0	0	0	,]
	шии	4 t D ts	₩ @	S - B	0	0	9 0	0	0	0 0	0	-	0	, -	-	0	0	0	-	0	0	9 0	,
	z ν ⊢ ν	14 4 D G	- - n	S ÷ B	-	0	90	0	0	0 0	0	٥		٥	0	1	0	-	0	-	- -		-
	αν⊢ν+	, n + 0 =	₩ =	s i b	-	0	0	0	0	0 0	0	0		, 0	0	ī	-	-	-		,	-	-
19 (19 (19 (19 (19 (19 (19 (19 (19 (19 (υ=	I W X H	H H	S - 6	0	0 0	0	0	0	0 0	0	0	0 0	, -	0	0	0	0	0	0	0	9 0	,
	ν κ ο ν) O + 10	Συ	S = 5	1	ᆔ,		0	0	0 0	0	0	0 0	, c	0	0	٥	0	0	0	0	> C	,
300 May 200 May	~ v ⊢ 		ы L	s == 5	1	0	0	0	0	0 0	0	0	0	, c	0	-	0	-	0	T	- 0	-	1
	z w + z	1 > + U =	# L	S - 0	1	0	0	0	0	0 0	0	0	0	0	, 0	0	0	0	0	0	0	> <	,
	>403Z	1>405	ے ب	0 - 0	1	н,			-		-			10) H	1	1	᠇	н	-	٦,	-	•
	m Z a	ו היאו		10 - D	0	0	- 0	0	0	0 0	0	0	0	-	0	0	0	•	0	0	- (5 C	,
	. O O T E O O) H - F R	۸۵	W D	0	0	0	0	0	0 0	0	0	0	۰	0	0	0	ᆔ	•	Ŧ	- (9 -	•
		∞ +- ∞	***	W D	0	0 (0	0	-		-	1	9	• -	-	1	1	н	1	0	0	3	•
		Q. 60 3	w o	10 - a	0	0	0 0	0	0	0 0	0	0		• •	0	0	0	0	0	0	0	5	>
	шZď	1U=	Į.	N - 0	0	0	0 =	0	0	0	0	1	0	-	1	0	٥	٥	П	0	0	-	2
	700) +- U =	1	S D	0	0	0 4	0	٥	0	0	0	0	9	0	0	0	0	0	٥	0	9 0	2
		80	13 8	W D	-	-	0 -		-	-	-	1	0	-	1-	=	П	П	ᅱ	-	-	<u>-1-</u>	1
		m z e	>+0) = + +	×	×	××	×	×	× >	×	×	× ×	< >	<×	×	×	×	×	×	×	- -	2
31	TONT	(T > F 0	& O	10-5	×	×	××	×	×	×	×	×	×	< >	\×	×	×	×	×	×	-	9	2
		٦	3 H C) O E 0	×	×	××	×	×	× >	×	×	× ;	4>	\×	H	0	-	0	×	× :	×××	4
シャカハミカ ト	l News	2 0 th 13	HAH	- I 10	×	×	××	×	×	×	×	×	× >	⁴	10	×	×	×	×	×	× :	× >	<
1017	B-+0=+	, м п д С	C 0	10 - 5	×	×	××	×	×	××	\×	×	×	1 0	0	×	×	×	×	×	× :	<u>* </u> *	<
Senothe Senothe	1 ወተተወ	2 D D 13	H D F	- I H	×	×	××	×	×	××	\×	×	٠ ;	4	0	×	×	×	×	×	×	× >	
теносет II		4 Z S	10 11 11	- w m F	×	×	<u> </u>	×	×	× •	0	×	×	1>	\×	×	×	×	×	×	×	<u> </u>	
N T B T O C T F	HZSHO	(4ZV	10 11 11	· w m F	×	×	××	×	1	<u> </u>	\×	×	×;	1	4×	×	×	×	×	×	×	<u> </u>	4
les .		×E	4 + >	* G H E	×	×	××	×	н	0	0	×	× ;	1	\×	×	×	×	×	×	×	*	1
	- O O H H C	- a - a - a	:0>	W 0	×	×	- -	×	×	× >	\×	×	×	1	(×	×	×	×	×	×	×	*	1
	F 4) w + H =	. 03.	· « D >	×	×	××	×	×	× >	×	×	× ;	1>	< ×	×	×	×	×	×	$\stackrel{\times}{+}$	<u> </u>	
					Ц							1	7									$\frac{1}{2}$	
				3.5				11					STAT		STAT					A			
				,5			A P	STAT						5	55		STAT	TAT	TAT	5	STA	SIS	3
							E E	E	ΑŢ	T t	A		ONIN			ES	E S	S	SO	SUL		: }	3
			Mile	OL OUTPUT	STAI		ATAC ATAC		STAT	STAT	į į	STAT	DAT			VRI	VRI	SX	SYL	XTRE	E		2
			6)0		RESET STAT	GO STAT	READ DATAIN STA	WRITE BITCHTR	JG SMC	36 SMC	JG SMC STA	SHIFT	SHIFT DATAINOUT	SHIET DATAINOUT STAT	SHIFT DATAINOUT	PAUSEWRITE STAT	PAUSEWRITE	CUSMC SYNC STAT	CUSMC SYNC STAT	RDYTOXTRESULT_STAT	WAITHSTRPLY_STAT	WALLESTEDLY STAT	
		<i>\$</i> **			RE	8	# H	į	8	9	2 2	Ŧ	5	5 2	5 6	PA	PA	3	3	8	3	3 3	

Inventor: Mohammed Ali AbdEl-Halim AbdEl-Wahid
Express Mail No.: EL874429377US / Date of Deposit: October 26, 2001
Title: DESIGN FOR TEST OF ANALOG MODULE SYSTEMS
Attorney's Matter No.: 1011-59137/RFS
Page 10 of 14

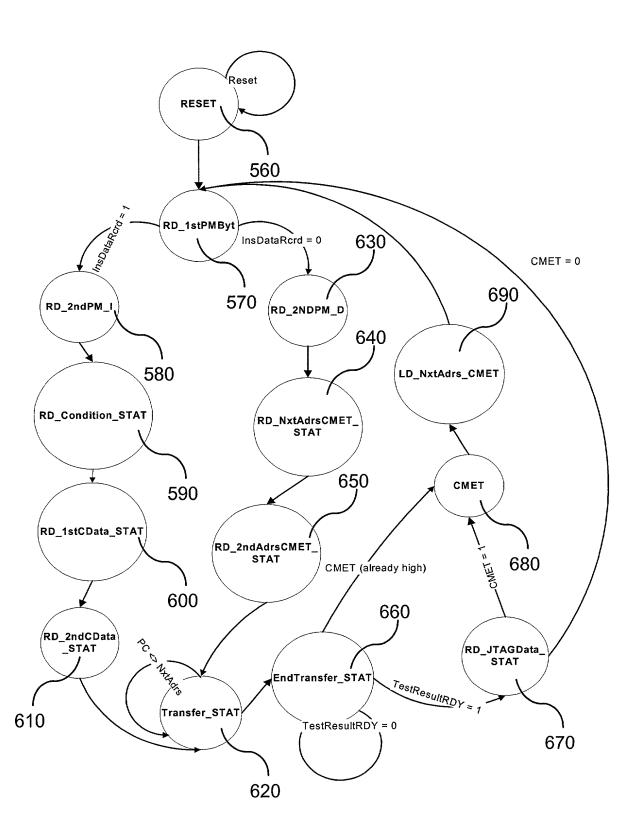


Inventor: Mohammed Ali AbdEl-Halim AbdEl-Wahid
Express Mail No.: EL874429377US / Date of Deposit: October 26, 2001
Title: DESIGN FOR TEST OF ANALOG MODULE SYSTEMS
Attorney's Matter No.: 1011-59137/RFS
Page 11 of 14

FIG. 9 60 470 80 DM Program COunter Pointer Adrs PROGRAM MEMORY High LOW PM Address 540 PC Byte Sel. Next Address 550 Control Words 480 PC & DPNTR Control DM 545 PM / JTAG Data MUX Data Memory Data PC Value Input Data From Host 490 Next Address **Next Address** Boundary Scan Data 2-to-4 Decoder Normal Checker Data 500 Latch Checker 520 530 No. Data Memory Control Control Bus Program Memory & JTAG Control 510 195 40 90 70 CMET JTAG CONDITION CHECKER Control Unit

Inventor: Mohammed Ali AbdEl-Halim AbdEl-Wahid
Express Mail No.: EL874429377US / Date of Deposit: October 26, 2001
Title: DESIGN FOR TEST OF ANALOG MODULE SYSTEMS
Attorney's Matter No.: 1011-59137/RFS
Page 12 of 14

FIG. 10



Attomey's Matter No.: 1011-59137/RFS Page 13 of 14 Inventor: Mohammed Ali AbdEl-Halim AbdEl-Wahid Express Mail No.: EL874429377US / Date of Deposit: October 26, 2001 Title: DESIGN FOR TEST OF ANALOG MODULE SYSTEMS

m cop e m -	0	0	H	0	0	0	0 0	0	0	0	0	H	н	ᆔ	н	0	0	0	0
₩₩, ₽₩ ₽₩ ₽₩	-	0	0	0	0	0	0 0	0	0	0	0	П	0	н	0	•	0	0	0
בסטייס אר סעם ומ – מ	•	0	0	0	0	0	0	0	0	0	0	1	ᆔ	н	ᆔ	-	0	0	0
ר ה א ה ה ל ס ≥ ה ס ≻ ט ט וע - ט	0	0	0	0	0	0		1-	1	0	1	0	•	0	0	0	н	-	0
ר ס א ר א כ ס א ר א ס ≻ וא − מ	0	0	0	0	0	0		. 0	1	0	0	0	0	0	•	0	-		0
	Sia		Sig	Sig	Sig	Sig	Sig			Sig	Sig	Sig	Sig	Sig	Sig	Sig	Sig	Sig	Sig
× € + H > N	XmtTvp	XmtTyp	XmtTyp	XmtTyp	XmtTyp	XmtTyp	XmtTyp	XmtTvp	XmtTyp	XmtTyp	XmtTyp_	XmtTyp	XmtTyp	XmtTyp	XmtTyp	XmtTyp	XmtTyp	XmtTyp	XmtTyp
	ľ	×	×	×	×				×	×	×	×	×	×	×	×	×	<u>~</u>	~
			=		_		N 1stData		=	_	=		_	_			_	_	_
ပြဲများက စာမ မေးများ မေးများ	.00.	.00	0.	00	.00"	CONDITTION	CONDITTON	8	00.	.00	00	.00.	00,,	00	00	00	0	.00.	.00
						3													
WK a V a h I O E k r I I D Q	-	H	1	1	-	0	0	, ,	-	н	-	1	Ŧ	н	1	1	П	1	Ŧ
O H M F A D O I O O P O Z D X I W - D	c	0	0	1	П	1	-	4 -	F	1	-	0	0	0	0	0	1	1	F
ang av≦ a × lu - a	-	-	1	1	н	н	-	-	1	1	н	1	1	1	1	ī	н	1	-
<u>ά</u> Σ ΙΌ ω Ι <i>Ο</i> — σ	Ţ-	0	0	0	0	0	+1 0	0	0	1	1	1	1	1	1	1	0	0	-
ΔΣ (≷ш (0)— п	-	-	1	ī	1	н		-	-	-	F	1	1	1	1	1	1	1	-
- Σ + O m + N - σ	-	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	H
ΔΣ Ιυш Ισ − δ	-	0	0	1	1	1	Ţ	-	1	Ŧ	1	0	0	0	0	0	. н	П	н
Z OΣ ISW IV≎ σ	C	0	0	1	1	1	1	4	Ħ	1	1	0	0	0	0	0	н		-
ДΣ (Ош (у) ≃ п	-	F	1	П	1	1		1 -	-	-	-	П	н	1	1	1		-	н
X E H + > a	×	×	×	×	×	×	×	< ×	×	×		1	1	0	0	×	×	×	×
, H, o' o → H c ± 5 1 × 0 >	*	×	×	×	×	X	×	< ×	×	П	0	×	×	×	×	×	×	×	×
X x 4 4 4 4 6 X + E - 14 X 8 5 + 4 A / 1 & O	>	×	×	×	×	×	×;	< -	0	×	×	×	×	×	×	×	×	×	×
оΣшь	>	=	0	×	×	×	×	< ×	×	×	×	×	×	×	×	×	×	×	×
												STAT	STAT	STAT	STAT		RD_NXTAdrsCMet_STAT	RD_ZndNXTAdrsCMet_S	TAT
No. of the last of		¥	Į,	RD_ZndPMemByt_I	2ndPMemByt_D	RD_Condition_STAT	RD_1stCData_STAT	Transfer STAT		TAT	TAT	RD JTAGINSDATA STAT	RD_JTAGINSDATA_STAT	RD_JTAGINSDATA_STAT	ATA		Met	ISCM	LD NXTAdrsCMet_STAT
Rator	TAT	IstPMemByt	RD 1stPMemByt	Mem	Mem	ition	ata		STAT	EndTransfer STAT	EndTransfer STAT	INSO	GSNI	INSD	RD_JTAGINSDATA	AT	drsC	XTAC	drsC
Leon Leon	DESET STAT	1stP	1stP	2ndP	2ndP	Cond	1stC	Transfer STA	Iransfer STAT	Frans	Frans	JTAG	JTAG	JIAG	JIAG	CMET_STAT	NXT	2nd	ξŽ
The state of the s	DEC	2	RD	B	RD G	B	2 8			End	End	8	8	8	8	8	RD	8	9
IG. 10A	_																		

Inventor: Mohammed Ali AbdEl-Halim AbdEl-Wahid
Express Mail No.: EL874429377US / Date of Deposit: October 26, 2001
Title: DESIGN FOR TEST OF ANALOG MODULE SYSTEMS
Attorney's Matter No.: 1011-59137/RFS
Page 14 of 14

FIG. 11

